REMARKS

Claims 1, 2, 4 - 15, 17 and 18 remain active in this application. By the above amendment, dependency of claim 14 has been revised and minor editorial revisions have been made in the syntax of claims 5 and 6. No new matter has been introduced into the application. The continued indication of allowability of claims 9 - 14 and 17 is noted with appreciation.

It is also respectfully pointed out that this response is in response to the *fifth action on the merits of this application* while the sole presently asserted ground of rejection is based on newly cited prior art of which the Examiner has been or should have been aware since the first action on the merits mailed December 13, 2001, because the newly cited prior art is incorporated by reference in prior art applied therein. Accordingly, supervisory review in accordance with M.P.E.P. §707.02(a) is respectfully requested.

The Examiner has objected to claim 14 due to the inadvertent introduction of a typographical error in dependency. This objection is respectfully traversed as moot in view of the above amendment to claim 14 which provides correction thereof. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claims 1 - 2, 4 - 8, 15 and 18 have been rejected under 35 U.S.C. §103 as being unpatentable over Fork '523 in view of Fork et al. '517. This ground of rejection is respectfully traversed for the reasons of record and the further remarks provided below.

Initially, it is noted that the previous grounds of rejection based on Fork '657 alone or in combination with Fork et al. '517 have been overcome and principal reliance is now placed on Fork '523 by the Examiner. As in Fork '657, Fork et al. '517 is also fully incorporated by reference in Fork '523. Therefore, as

with Fork '657, the subject matter of Fork et al. '517 is literally as well as constructively present in Fork '523 and the principal issues remain, as in the previous office action: 1.) whether or not Fork '523, including the subject matter of Fork et al. '517, contains teachings or suggestions which answer the claim recitations or contains evidence of the level of ordinary skill in the art which would support a conclusion of obviousness of the claimed subject matter and 2.) whether or not Fork '523 *per se* can be modified in accordance with Fork et al '517 *per se* in accordance with the teachings or suggestions of either without loss of intended function (in which case, the proposed modification would be improper under In re Gordon, previously cited and discussed). As in the previous response, reference to Fork '523 *per se* or Fork et al. '517 *per se* will be used to indicate reference to the explicit disclosure of each respective document exclusive of the incorporations by reference.

It is Applicants' basic position that, while Fork '523 is more relevant to the present invention than Fork '657, previously applied against the claims alone or in combination with Fork et al. '517, that the teachings and suggestions of the combined disclosures are considerably more limited than the Examiner asserts. The limitations of the combined teachings and/or suggestions are particularly evident when it is appreciated that the various patents to Fork and Fork et al. are directed to various aspects and possible features of an optical printer head which may be used in some combinations while some disclosed possible variants are inconsistent with each other and cannot be used in combination or present particular constraints or limitations on the print head or its operation. Of particular importance in considering the propriety of the present ground of rejection is the concern in both Fork '523 and Fork et al. '517 in regard to the trade-

off between print head resolution and the functionality of drive circuitry which may be integrated with the light-emitter array, particularly in regard to provision of cumulative exposure to allow the usable lifetime of the light-emitters to be extended by reducing light emission levels.

That is, Fork '523 is primarily concerned with providing a resolution of 300 dots per inch (dpi) rather than a lower resolution (e.g. 200 dpi) which would be imposed by bonding density if the vertical shift registers were formed as peripheral devices. Note, in particular, the constraint on dpi imposed by the number and density of drive lines explicitly noted at column 8, lines 20 - 30. Thus Fork '523 proposes to form respective *vertical* shift register stages *under* respective pixels/light-emitters. However, to do so consistent with adequate performance of TFT polysilicon transistors of sufficiently small size imposes constraints on the functionality of the shift registers which can be provided such that no horizontal shift register can be similarly provided (since substantially the entire pixel area is consumed by the required twelve shift register stage transistors and the driver transistor of the vertical shift register stages).

Thus, contrary to the Examiner's assertion, any horizontal scanning circuit is specifically and necessarily excluded from integration with the vertical shift register and the light-emitter array formed thereover. Further, any grey scale effects can be produced, in accordance with Fork '523, only by analog pixel drive (see column 10, lines 4 - 13) since there is no room for transistors for interrupting cumulative exposure in accordance with a controllable number of pixel exposures.

Similarly, Fork et al. '517 is directed to producing a grey scale by controlling the number of sequential exposures of an area of a light-sensitive

medium by providing for rewriting of the shift register data at any line or vertical shift register stage but concedes (while acknowledging the much higher data switching rates that would be required) that such a function cannot be achieved consistent with a high resolution light emitting array except by using "*peripheral* data multiplexing circuitry" (emphasis added) due to the requirement of a memory cell and a current source and that higher resolution is possible when only two selection and drive transistors are integrated with each pixel as opposed to including a shift register stage at the pixel (see column 7, lines 42 - 58); again acknowledging the requirement for analog drive to produce a grey scale to the exclusion of producing a grey scale by controlling the *number*, rather than *analog* intensity, of cumulative partial exposures.

Further, while Fork '523 is substantially silent as to the distribution of data signals in the horizontal direction (and it is respectfully submitted that the Examiner is clearly incorrect in asserting that elements 62, 64 and 66 constitute a horizontal shift register, as can be confirmed from column 4, lines 51 - 65), Fork et al. '517 teaches or suggests only buffering in a peripheral circuit 36 responsive to address generator 38 and counter 40 and thus does not teach or suggest horizontal scanning much less with a shift register and certainly not integrated with the light-emitter array or, for that matter, vertical scanning circuitry.

More specifically, the basic invention, as recited in the independent claims 1 and 15 provides a print head comprising a two-dimensional array of light emitters, a horizontal scanning circuit and a vertical scanning circuit wherein all three of these elements are formed on the same insulating substrate and both the horizontal and vertical scanning circuits are

formed of poly-crystal thin-film transistors. By doing so, high resolution can be provided consistent with a compact and economical print head structure which would otherwise be limited in resolution by connection wiring and/or bonding density. See page 6, lines 4 - 9. This problem is acknowledged at column 8, lines 20 - 30 of Fork '523 (noting the impracticality of providing shift registers outside the array consistent with high resolution as well as indicating a criticality of transistor technology at column 6, lines 33 - 38, even for the slow scan shift rate, and number of clock, data and voltage supply lines at column 5, lines 38 - 43, relative to pixel area). The problem is also acknowledged at column 7, lines 42 - 58, of Fork et al. '517 (noting that the higher resolution cannot be obtained using shift registers in the light emitter array consistent with production of a grey scale by cumulative exposure of a given low intensity because of the greater required number of transistors and greater required switching speed) and is addressed by the proposed addition of "*peripheral* data multiplexing circuitry" (emphasis added) even though the multiplexing circuitry can evidently be formed using the same process steps as the pixel circuitry but, in any case, cannot be formed with the vertical shift register due to lack of additional available chip area.

It should be noted that the shift registers referred to in these passages of Fork '523 and Fork et al. '517 provide data shifting only in the slow scan or vertical scanning direction and scanning in the horizontal direction to deliver data to each of the shift registers (e.g. 62, 64, 66 of Fork '523) must operate at a much high scan rate (e.g. the vertical shift rate multiplied by the number of pixels in a scan line) as noted at column 5, line 52, to column 6, line 19, of Fork et al '517. That is, contrary to the Examiner's assertion, elements 62, 64 and 66 of Fork

'523 do not constitute a horizontal scanning means but, rather, are shift registers (or the initial stages thereof) for slow scanning in the vertical direction and, while Fork '523 forms the light emitting array over the shift register circuits for scanning in the vertical direction, Fork '523 *per se* is substantially silent as to formation of a horizontal scanning means or shift register on the same insulating substrate with the light-emitting array and the vertical scanning shift registers (merely assuming data distribution in the horizontal direction) while admitting criticality of connection number and spacing and transistor technology to support avoidance of limitation on pixel pitch and printer resolution due to connection and bonding density. Fork et al. '517, as previously pointed out, does not teach or suggest horizontal scanning circuitry formed on the same substrate with the light-emitting array and the vertical scanning circuit but only buffering in a peripheral circuit for which no integration with other circuits or light emitters is proposed while integration of any circuitry beyond driver and selection transistors with the light-emitters is noted to be inconsistent with desired pixel pitch.

Thus, if Fork '523 teaches anything of relevance to the constitution or formation of a horizontal scanning circuit (even through the various incorporations by reference contained therein) it is the inference (from the demonstration of operability of polysilicon TFT transistors of suitable size at the much lower, slow scan data rate, as distinguished from amorphous TFT transistors which would be required to be of unsuitably large size in order to operate) that the polysilicon TFT technology transistors of the vertical scanning shift registers may not be sufficient (or, at least, were not recognized as sufficient as of the filing date of Fork '523) for accommodating the

required horizontal data distribution data rates and cannot be formed using the same semiconductor technology on the same substrate as the light-emitting array and the vertical scanning circuits. The same inference is also reached from the substantial filling of the pixel space with transistors required by each vertical scan shift register stage and with stringent constraints on connection pitches. Therefore, it is respectfully submitted that the combination of Fork '523 and Fork et al. '517 does not answer the explicitly recited subject matter of even independent claims 1 or 15 since it does not teach, suggest or enable the formation of a horizontal scanning circuit on the same substrate as the light-emitting array and the vertical scanning circuit.

Moreover, the combination of Fork '523 and Fork et al. '517 does not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness of the claimed subject matter, taken as a whole, since Fork et al. '517 *per se* does not provide a solution to the tradeoff, acknowledged in Fork '523 with indication of criticality of transistor technology and shift register functionality, between maximum pixel pitch (e.g. 300 dpi which can be achieved in accordance with Fork et al. '517 by forming only drive transistors beneath the OLEDs but which is precluded without *peripheral* data multiplexing circuits or if shift register scanning circuits are provided as noted at column 7, lines 42 - 58). In this regard, it should be appreciated that the filling of pixel area with vertical scanning structure to the exclusion of other circuitry is the technique by which Fork '523 provides a solution to the problem of providing high resolution consistent with limitation of light-emitter brightness through cumulative exposure to extend the functional lifetime of the light-emitters while tolerating, rather than solving, the attendant

problems and constraints in regard to vertical shift register functionality, limitation of grey scale production techniques, transistor technology and horizontal data distribution consistent with comparable resolution in the horizontal direction. There is no recognition is either Fork '523 or Fork et al '517 that integration of both horizontal and vertical scanning circuits with a pixel array (but not necessarily integration of shift register stages under respective pixel areas provides a solution to the constraint on pixel pitch imposed by wire bond density or that poly-crystal TFT transistors of sufficiently small size are adequate for horizontal scanning circuitry, much less that the latter supports the practical realization of the former and, in combination, supports the meritorious effects of the present invention.

Therefore, it is respectfully submitted that Fork '523 and Fork et al '517 taken separately or together, do not teach or suggest the claimed print head in which the light-emitter array a vertical scanning circuit and a horizontal scanning circuit are all provided and formed of poly-crystal TFT transistors on the same insulating substrate. Further, these references do not even acknowledge the possibility of such a combination or realization of the meritorious effects achievable by such a combined structure to provide a compact and economical print head which can be manufactured at high yield (and which is not constrained as to techniques of producing a grey scale consistent with low light emission levels for extending usable life of light-emitters by cumulative exposure with a variable *number* of sequential exposures. There is no disclosed alternative consistent with high pixel pitch to forming the vertical drive transistors or the vertical shift register stages directly under the pixels or any recognition that constraints on resolution and scanning circuit functionality due to connection/bonding density

can be avoided by formation of all circuits on the same substrate to avoid the need for bonding of connections to peripheral circuits. Therefore, it is also respectfully submitted that Fork '523 and Fork et al. do not provide evidence of a level of ordinary skill in the art do not and cannot provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness the Examiner has asserted since these reference do not lead to an expectation of success in achieving the meritorious effects of the invention by providing the claimed structures comprising poly-crystal TFT transistors formed on the same insulating substrate with the light-emitting array.

Further, at best, the modification of Fork '523 in accordance with Fork et al. '517 which the Examiner proposes is not only incorrect as to the content of Fork '523 (e.g. asserting that elements 62, 64 and 66 comprise a horizontal scanning arrangement) and Fork et al. '517 (e.g. asserting that buffer 36 is a scanning arrangement or that it is other than a separately formed peripheral circuit) but would result in a structure which is explicitly disclosed to be undesirable (e.g. due to resolution or operational constraints) and would involve combining of features noted to be incompatible in a structure which Fork '523 and/or Fork et al. '517 considers to be desirable. Therefore the proposed modification is not only grounded in error as to the content of each reference *per se* but improper under In re Gordon, *supra*. Moreover, the claimed structure supports production of a grey scale in a manner which the Examiner concedes to be novel by the allowance of dependent claims directed thereto and which would not be supported by the proposed modified structure as acknowledged by both Fork '523 (which acknowledges the necessity of analog drive to produce a grey scale) and Fork et al. '517

(which acknowledges that high resolution cannot be achieved with a scanning shift register having a functionality which supports alteration of the number of cumulative exposures, even if scanning is provided for only the vertical direction. Therefore, it also logically follows that the claimed combination provides functions not available from the proposed modified structure (and explicitly disclosed to be unavailable from any structure resulting from a properly proposed modification of the combined teachings of the references) and the invention, as claimed, must therefore be regarded as novel and patentably distinguished therefrom.

Accordingly, it is respectfully submitted that the rejection of claims 1, 2, 4 - 8, 15 and 18 is clearly in error and that the Examiner has not made and cannot make a *prima facie* demonstration of obviousness of any claim included in this sole remaining ground of rejection. Further, it is clear that the teachings and suggestions of the combined disclosures are considerably more limited than the Examiner asserts and, even if properly combinable, do not answer the recitations of the claims. Therefore, it is respectfully requested that this ground of rejection be reconsidered and withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a

conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

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